AMENDMENTS TO THE ABSTRACT

Please substitute the following paragraph for the abstract now appearing in the currently filed specification:

A computer implemented parallel processing method for performing a logic simulation. The method includes representing signals on a line over a time period as a bit sequence, and evaluating gate outputs of logic gates including an evaluation of any inherent delay by comparing bit sequences of inputs of the logic gates to a predetermined series of bit patterns and in which logic gates whose outputs have changed over the time period are identified during the evaluation of the gate outputs as real gate changes and only the logic gates having the real gate changes are propagated to respective fan out gates of the logic gates having the real gate changes. The method also includes storing in word form in an associative memory mechanism a history of gate input signals by compiling a hit list register of logic gate state changes, generating an address for each hit in the hit list via a multiple response resolver forming a part of the associative memory mechanism, and then scanning and transferring results on the hit list to an output register for subsequent use, and dividing an associative register into separate smaller associative sub-registers, allocating one type of logic gate to each associative sub-register, each of which associative sub-registers has corresponding sub-registers connected thereto, and carrying out gate evaluations and tests in parallel on each associative sub-register.